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In re Patent Application of
GENDRIER ET AL.
Serial No. 10/511,712
Filed: OCTOBER 15, 2004

In the Claims:

This listing of claims replaces all prior versions and listing of claims in the application.

Claims 1-33 (Canceled).

34. (Currently amended) A semiconductor memory device comprising:

at least one electrically erasable and programmable non-volatile memory cell including

a layer of gate material,

a floating-gate transistor including a floating gate defined in the layer of gate material, and further including source, drain and channel regions defining a control gate,

a first active zone, and

a second active zone incorporating the control gate and electrically isolated from the first active zone,

a dielectric zone between a first part of the layer of gate material and the first active zone;

the dielectric zone defining a transfer zone for transferring, during erasure of the memory cell, charges stored in the floating gate to the first active zone.

35. (Previously presented) The device according to Claim 34, wherein the capacitance of the transfer zone is less than or equal to 30% of a total capacitance between the layer of gate material and the active zones of the memory cell.

36. (Previously presented) The device according to Claim 34, wherein the floating-gate comprises an annular gate defined in the layer of gate material, and wherein the layer of gate material includes a linking part between the first part and the annular gate.

37. (Previously presented) The device according to Claim 34, wherein the first active zone and the second active zone are electrically isolated from each other by reverse-biased PN junctions.

38. (Previously presented) The device according to Claim 37, wherein the first active zone and the second active zone are electrically isolated from each other on a surface of the memory cell by an isolation region.

39. (Previously presented) The device according to Claim 38, wherein the first active zone is disposed in a first substrate region having a first type of conductivity, the second active zone is disposed in a second substrate region having the first type of conductivity, the first substrate region and the second substrate region are separated by a third substrate region having a second type of conductivity, different from the first, and wherein the isolation region extends between the first substrate region and the second substrate region and includes an aperture in a contact zone in the third semiconductor region.

40. (Previously presented) The device according to Claim 39, wherein the first substrate region includes, on the surface, a contact zone having the first type of conductivity.

41. (Previously presented) The device according to Claim 37, wherein the first active zone is disposed in a first substrate region having a first type of conductivity, the second active zone is disposed in a second substrate region having the first type of conductivity, the first substrate region and the second substrate region are separated by a third substrate region having a second type of conductivity, different from the first, and wherein the layer of gate material extends above the three substrate regions without overlapping the isolation region.

42. (Previously presented) The device according to Claim 41, wherein the first substrate region includes, on the surface, a contact zone having the first type of conductivity.

43. (Previously presented) The device according to Claim 42, wherein the first substrate region further includes a surface zone having the second type of conductivity and extending around the transfer zone, the surface zone being electrically connected to the contact zone.

44. (Previously presented) The device according to Claim 34, wherein the floating gate transistor comprises a PMOS transistor.

45. (Previously presented) The device according to Claim 34, wherein the at least one memory cell comprises a plurality of memory cells defining a memory plane, each memory cell including an access transistor.

46. (Previously presented) The device according to Claim 34 further comprising a bias device possessing a memory cell programming state, a memory cell read state and a memory cell erase state, wherein the bias device is for applying, in each of the states, predetermined voltages to the source, the drain and the substrate of the floating gate transistor and to the first active zone, and wherein, in the erase state, the bias device causes Fowler-Nordheim erasing by applying a voltage to the first active zone much higher than voltages applied to the source, drain and substrate regions of the floating gate transistor.

47. (Previously presented) The device according to Claim 46, wherein in the erase state, the bias device applies equal voltages to the source, drain and substrate regions of the floating gate transistor.

48. (Previously presented) The device according to Claim 46, wherein in the programming state, the bias device causes hot-carrier programming within the floating gate.

49. (Previously presented) The device according to Claim 46 wherein, in the programming state, the bias device causes Fowler-Nordheim programming by applying equal voltages

to the source, drain and substrate regions of the floating gate transistor that are much higher than voltages applied to the first active zone.

50. (Previously presented) The device according to Claim 46, wherein, in the read state, the drain/source voltage difference is limited to about 1 volt.

51. (Previously presented) The device according to Claim 34, wherein the at least one memory cell comprises a plurality of memory cells defining a memory plane, each memory cell including an access transistor; wherein the access transistor of a memory cell flanked by two adjacent memory cells located in a same column as the memory cell includes a first elementary access transistor specifically associated with the memory cell and second and third elementary access transistors respectively common to two access transistors assigned to the two adjacent memory cells respectively; wherein a source of the access transistor forms a source of the first elementary access transistor while a drain of the first elementary access transistor forms part of the source of the floating-gate transistor of the memory cell; and further comprising a bias device for selecting at least one memory cell in program mode and in read mode and for erasing the memory plane via blocks of memory cells.

52. (Previously presented) The device according to Claim 51, wherein the bias device is for applying a same source bias voltage to the respective sources of the access

transistors of the memory cells of any one column respectively, a same gate bias voltage to the respective gates of the access transistors of the memory cells of the same column respectively and the same erase voltage to the respective first active zones of the memory cells of at least the same column.

53. (Previously presented) The device according to Claim 51, wherein the access transistor of a memory cell partially surrounds the floating gate transistor of the memory cell.

54. (Previously presented) The device according to Claim 53, wherein each column of memory cells has a layer of gate material including a main part extending in the direction of the column along and opposite the floating-gate transistors of the memory cells; wherein the gate of the first elementary access transistor of an access transistor of a memory cell includes a portion of the main part of the layer of gate material which is located opposite the floating-gate transistor of the memory cell; wherein the layer of gate material includes, within each memory cell, a second elementary portion connected to the main part and extending approximately perpendicular to the main part on one side of the floating-gate transistor of the memory cell, to form part of the gate of the second elementary transistor of the access transistor, and a third elementary portion connected to the main part and extending approximately perpendicular to the main part on the other side of the floating-gate transistor of

the memory cell, to form part of the gate of the third elementary transistor of the access transistor; and wherein the second elementary portion associated with a memory cell defines the third elementary portion associated with one of the two adjacent memory cells, and the third elementary portion associated with the memory cell defines the second elementary portion associated with the other of the two adjacent memory cells.

55. (Previously presented) The device according to Claim 51, wherein the bias device possesses a programming state to program a memory cell, a read state to read a memory cell and an erase state to erase at least one column of memory cells; wherein the bias device is for applying, in each of the states, predetermined voltages to the sources and the gates of the access transistors, and to the drains and the substrates of the floating-gate transistors of the memory cells and to the first active zones; and wherein, in the erase state, the bias device causes Fowler-Nordheim erasing by applying a voltage to the first active zones that is much higher than voltages applied to the source regions of the access transistors, and to the drain and substrate regions of the floating-gate transistors.

56. (Previously presented) The device according to Claim 55, wherein to access a memory cell in read mode or in programming mode, the bias device turns on the access transistors of the memory cells belonging to the same column as that of the memory cell, applies an identical voltage to

the source of the access transistor and the drain of the floating-gate transistor of each memory cell of the column different from the memory cell, and turns off the access transistors of the memory cells belonging to a column other than that of the memory cell.

57. (Previously presented) The device according to Claim 56, wherein the bias device programs a memory cell that has undergone erasure, the floating gate transistor of which cell is a PMOS transistor, by carrying out hot-electron programming on the transistor in two successive steps to firstly compensate for any residual positive charges present in the floating gate transistor and then to carry out optimum programming.

58. (Previously presented) The device according to Claim 57, wherein in a first step of the two steps, the bias device compensates for any residual positive charges present in the floating gate transistor by applying a compensation voltage to the contact zone of the first active zone.

59. (Previously presented) The device according to Claim 58, wherein the compensation voltage is less than or equal to 0 volts and greater than about -500 mV.

60. (Previously presented) The device according to Claim 36, wherein the at least one memory cell comprises a plurality of memory cells defining a memory plane, each memory cell including an access transistor; wherein the access

transistor of a memory cell comprises a gate extending perpendicular to the linking part and on the opposite side from the linking part with respect to the annular gate, wherein the source of the access transistor comprises a source contact, the drain of the access transistor forms part of the source of the floating-gate transistor of the memory cell, and the drain of the floating-gate transistor is electrically connected to the second active zone.

61. (Previously presented) The device according to Claim 60, wherein the source contacts of the access transistors of the memory cells of any one column of the memory plane are connected together, the first active zones of the memory cells of any one column of the memory plane are connected together, the gates of the access transistors of the memory cells of any one line of the memory plane are connected together, and the corresponding gate contacts are connected together by a line metallization, the drains of the floating-gate transistors of the memory cells of any one line of the memory plane are connected together to form another line metallization; and further comprising a bias device for selecting at least one memory cell in programming mode and for programming the at least one memory cell by Fowler-Nordheim programming.

62. (Previously presented) The device according to Claim 61, wherein the bias device selects a memory cell of the memory plane and programs the memory cell by applying a sufficient potential difference between the drain of the

floating-gate transistor of the memory cell and the first active zone of the memory cell.

63. (Previously presented) The device according to Claim 61, wherein the bias device is for erasing the memory plane in its entirety.

64. (Previously presented) The device according to Claim 63, wherein the bias device erases the memory plane in its entirety by applying a high voltage to the first active zones of the memory cells and by applying a zero voltage to other contacts of the memory cells.

65. (Previously presented) The device according to one of Claim 61, wherein the bias device is for reading the memory plane line by line by turning on the access transistors of the memory cell of a line and by turning off the access transistors of the memory cells of other lines.

66. (Previously presented) The device according to Claim 61, wherein the memory plane defines at least one of an EEPROM type memory and a FLASH type memory.

67. (Previously presented) An integrated circuit comprising a semiconductor memory device according to Claim 34.

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68. (Currently amended) A method of making a semiconductor memory device comprising:

providing at least one electrically erasable and programmable non-volatile memory cell including

a layer of gate material,

a floating-gate transistor including a floating gate defined in the layer of gate material, and further including source, drain and channel regions defining a control gate,

a first active zone, and

a second active zone incorporating the control gate and electrically isolated from the first active zone,

a dielectric zone between a first part of the layer of gate material and the first active zone;

the dielectric zone defining a transfer zone for transferring, during erasure of the memory cell, charges stored in the floating gate to the first active zone.

69. (Previously presented) The method according to Claim 68, wherein the capacitance of the transfer zone is less than or equal to 30% of a total capacitance between the layer of gate material and the active zones of the memory cell.

70. (Previously presented) The method according to Claim 68, wherein the floating-gate comprises an annular gate defined in the layer of gate material; and providing the layer of gate material with a linking part between the first part and the annular gate.

71. (Previously presented) The method according to Claim 68, further comprising electrically isolating the first active zone and the second active zone from each other by reverse-biased PN junctions.

72. (Previously presented) The method according to Claim 71, further comprising electrically isolating the first active zone and the second active zone from each other on a surface of the memory cell with an isolation region.

73. (Previously presented) The method according to Claim 72, wherein the first active zone is disposed in a first substrate region having a first type of conductivity, the second active zone is disposed in a second substrate region having the first type of conductivity, the first substrate region and the second substrate region are separated by a third substrate region having a second type of conductivity, different from the first, and wherein the isolation region extends between the first substrate region and the second substrate region and includes an aperture in a contact zone in the third semiconductor region.

74. (Previously presented) The method according to Claim 73, further comprising providing a contact zone having the first type of conductivity on the surface of the first substrate region.

75. (Previously presented) The method according to Claim 71, wherein the first active zone is disposed in a first substrate region having a first type of conductivity, the second active zone is disposed in a second substrate region having the first type of conductivity, the first substrate region and the second substrate region are separated by a third substrate region having a second type of conductivity, different from the first, and wherein the layer of gate material extends above the three substrate regions without overlapping the isolation region.

76. (Previously presented) The method according to Claim 75, further comprising providing a contact zone having the first type of conductivity on the surface of the first substrate region.

77. (Previously presented) The method according to Claim 76, further comprising providing a surface zone having the second type of conductivity and extending around the transfer zone in the first substrate region; and electrically connecting the surface zone to the contact zone.

78. (Previously presented) The method according to Claim 68, wherein the floating gate transistor comprises a PMOS transistor.

79. (Previously presented) The method according to Claim 68, wherein the at least one memory cell comprises a plurality of memory cells defining a memory plane; further

comprising providing each memory cell with an access transistor.

80. (Previously presented) The method according to Claim 68 further comprising providing a bias device possessing a memory cell programming state, a memory cell read state and a memory cell erase state, wherein the bias device is for applying, in each of the states, predetermined voltages to the source, the drain and the substrate of the floating gate transistor and to the first active zone, and wherein, in the erase state, the bias device causes Fowler-Nordheim erasing by applying a voltage to the first active zone much higher than voltages applied to the source, drain and substrate regions of the floating gate transistor.

81. (Previously presented) The method according to Claim 80, wherein in the erase state, the bias device applies equal voltages to the source, drain and substrate regions of the floating gate transistor.

82. (Previously presented) The method according to Claim 80, wherein in the programming state, the bias device causes hot-carrier programming within the floating gate transistor.

83. (Previously presented) The method according to Claim 80 wherein, in the programming state, the bias device causes Fowler-Nordheim programming by applying equal voltages to the source, drain and substrate regions of the floating

gate transistor that are much higher than voltages applied to the first active zone.

84. (Previously presented) The method according to Claim 80, wherein, in the read state, the drain/source voltage difference is limited to about 1 volt.

85. (Previously presented) The method according to Claim 68, wherein the at least one memory cell comprises a plurality of memory cells defining a memory plane; further comprising providing each memory cell with an access transistor; wherein the access transistor of a memory cell flanked by two adjacent memory cells located in a same column as the memory cell includes a first elementary access transistor specifically associated with the memory cell and second and third elementary access transistors respectively common to two access transistors assigned to the two adjacent memory cells respectively; wherein a source of the access transistor forms a source of the first elementary access transistor while a drain of the first elementary access transistor forms part of the source of the floating-gate transistor of the memory cell; and further comprising a bias device for selecting at least one memory cell in program mode and in read mode and for erasing the memory plane via blocks of memory cells.

86. (Previously presented) The method according to Claim 85, wherein the bias device is for applying a same source bias voltage to the respective sources of the access

transistors of the memory cells of any one column respectively, a same gate bias voltage to the respective gates of the access transistors of the memory cells of the same column respectively and the same erase voltage to the respective first active zones of the memory cells of at least the same column.

87. (Previously presented) The method according to Claim 85, wherein the access transistor of a memory cell partially surrounds the floating gate transistor of the memory cell.

88. (Previously presented) The method according to Claim 87, wherein each column of memory cells has a layer of gate material including a main part extending in the direction of the column along and opposite the floating-gate transistors of the memory cells; wherein the gate of the first elementary access transistor of an access transistor of a memory cell includes a portion of the main part of the layer of gate material which is located opposite the floating-gate transistor of the memory cell; wherein the layer of gate material includes, within each memory cell, a second elementary portion connected to the main part and extending approximately perpendicular to the main part on one side of the floating-gate transistor of the memory cell, to form part of the gate of the second elementary transistor of the access transistor, and a third elementary portion connected to the main part and extending approximately perpendicular to the main part on the other side of the floating-gate transistor of

the memory cell, to form part of the gate of the third elementary transistor of the access transistor; and wherein the second elementary portion associated with a memory cell defines the third elementary portion associated with one of the two adjacent memory cells, and the third elementary portion associated with the memory cell defines the second elementary portion associated with the other of the two adjacent memory cells.

89. (Previously presented) The method according to Claim 85, wherein the bias device possesses a programming state to program a memory cell, a read state to read a memory cell and an erase state to erase at least one column of memory cells; wherein the bias device is for applying, in each of the states, predetermined voltages to the sources and the gates of the access transistors, and to the drains and the substrates of the floating-gate transistors of the memory cells and to the first active zones; and wherein, in the erase state, the bias device causes Fowler-Nordheim erasing by applying a voltage to the first active zones that is much higher than voltages applied to the source regions of the access transistors, and to the drain and substrate regions of the floating-gate transistors.

90. (Previously presented) The method according to Claim 85, wherein to access a memory cell in read mode or in programming mode, the bias device turns on the access transistors of the memory cells belonging to the same column as that of the memory cell, applies an identical voltage to

the source of the access transistor and the drain of the floating-gate transistor of each memory cell of the column different from the memory cell, and turns off the access transistors of the memory cells belonging to a column other than that of the memory cell.

91. (Previously presented) The method according to Claim 90, wherein the bias device programs a memory cell that has undergone erasure, the floating gate transistor of which cell is a PMOS transistor, by carrying out hot-electron programming on the transistor in two successive steps to firstly compensate for any residual positive charges present in the floating gate transistor and then to carry out optimum programming.

92. (Previously presented) The method according to Claim 91, wherein in a first step of the two steps, the bias device compensates for any residual positive charges present in the floating gate transistor by applying a compensation voltage to the contact zone of the first active zone.

93. (Previously presented) The device according to Claim 92, wherein the compensation voltage is less than or equal to 0 volts and greater than about -500 mV.

94. (Previously presented) The method according to Claim 70, wherein the at least one memory cell comprises a plurality of memory cells defining a memory plane; further comprising providing each memory cell with an access

transistor; wherein the access transistor of a memory cell comprises a gate extending perpendicular to the linking part and on the opposite side from the linking part with respect to the annular gate; wherein the source of the access transistor comprises a source contact, the drain of the access transistor forms part of the source of the floating-gate transistor of the memory cell, and the drain of the floating-gate transistor is electrically connected to the second active zone.

95. (Previously presented) The device according to Claim 94, wherein the source contacts of the access transistors of the memory cells of any one column of the memory plane are connected together, the first active zones of the memory cells of any one column of the memory plane are connected together, the gates of the access transistors of the memory cells of any one line of the memory plane are connected together, and the corresponding gate contacts are connected together by a line metallization, the drains of the floating-gate transistors of the memory cells of any one line of the memory plane are connected together to form another line metallization; and further comprising a bias device for selecting at least one memory cell in programming mode and for programming the at least one memory cell by Fowler-Nordheim programming.

96. (Previously presented) The method according to Claim 95, wherein the bias device selects a memory cell of the memory plane and programs the memory cell by applying a sufficient potential difference between the drain of the

floating-gate transistor of the memory cell and the first active zone of the memory cell.

97. (Previously presented) The method according to Claim 95, wherein the bias device is for erasing the memory plane in its entirety.

98. (Previously presented) The method according to Claim 97, wherein the bias device erases the memory plane in its entirety by applying a high voltage to the first active zones of the memory cells and by applying a zero voltage to other contacts of the memory cells.

99. (Previously presented) The method according to Claim 95, wherein the bias device is for reading the memory plane line by line by turning on the access transistors of the memory cell of a line and by turning off the access transistors of the memory cells of other lines.

100. (Previously presented) The method according to Claim 95, wherein the memory plane defines at least one of an EEPROM type memory and a FLASH type memory.